**Important Instructions to examiners:**

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate’s answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate’s understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

<table>
<thead>
<tr>
<th>Q. No.</th>
<th>Sub Q. N.</th>
<th>Answers</th>
<th>Marking Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A</td>
<td>Attempt any SIX:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>List different operating regions of transistor.</td>
<td>12- Total Marks</td>
</tr>
<tr>
<td>a</td>
<td></td>
<td>Ans: Operating regions of transistor:-</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Operating Region</td>
<td>I_B or V_CE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cut off</td>
<td>I_B = very small</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Saturation</td>
<td>V_CE = Very small</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Active</td>
<td>V_CE = Moderate</td>
</tr>
<tr>
<td>b</td>
<td></td>
<td>Define the term stability factor.</td>
<td>2M</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ans: Stability factor</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>It is defined as the rate of change of collector current I_C with respect to the collector base leakage current I_CO, keeping both the current I_B and the current gain ( \beta ) constant.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[ S = \frac{\partial I_C}{\partial I_CO} = \frac{dI_C}{dI_CO} = \frac{\Delta I_C}{\Delta I_CO} ]</td>
<td>2M</td>
</tr>
<tr>
<td>c</td>
<td>Draw the symbol of n-channel and p-channel JFET.</td>
<td>2M</td>
<td></td>
</tr>
<tr>
<td>---</td>
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<td>---</td>
<td></td>
</tr>
<tr>
<td>Ans:</td>
<td>Symbol of n-channel and p-channel JFET:</td>
<td>1M each</td>
<td></td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="Schematic Symbol" /></td>
<td></td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>d</th>
<th>List the types of amplifier coupling.</th>
<th>2M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ans:</td>
<td>Types of amplifier coupling: (ANY TWO)</td>
<td>1M each</td>
</tr>
<tr>
<td></td>
<td>2. Transformer coupling</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3. Direct coupling</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>e</th>
<th>Define intrinsic stand-off ratio of UJT.</th>
<th>2M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ans:</td>
<td>Intrinsic stand-off ratio:</td>
<td>(Definition: 1M, Equation: 1M)</td>
</tr>
<tr>
<td></td>
<td>It is defined as the ratio of the $R_{B1}$ (base resistance 1) to the inter-base resistance $R_{BB}$.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\eta = \frac{R_{B1}}{R_{BB}} = \frac{R_{B1}}{R_{B1} + R_{B2}}$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>f</th>
<th>State the need of voltage regulator.</th>
<th>2M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ans:</td>
<td>NEED OF VOLTAGE REGULATORS:-</td>
<td>2M</td>
</tr>
<tr>
<td></td>
<td>DC voltage obtained by using rectifier and filter is not constant and may vary depending upon supply variations. This DC voltage may result in an error or may damage other electronic devices or circuits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>e.g.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1. In oscillators it may lead to phase shift.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2. In amplifiers it may lead to change in voltage gain or power gain.</td>
<td></td>
</tr>
</tbody>
</table>
3. It may lead to calibration error in measuring instruments.
4. It may produce distortions in output of audio and video amplifiers.
Hence to avoid these errors DC voltage regulators are necessary to keep the output DC voltage constant.

g  Define efficiency of power amplifier.  
**Ans:**

**Definition:**
Efficiency of power amplifier is defined as the ratio of r. m. s. output power dissipated in the load to the total DC power taken from the supply source.

**Formula:**

\[
\eta \% = \frac{P_{out}}{P_{DC}} \times 100
\]

Where:
- \( \eta \% \) – is the efficiency of the amplifier.
- \( P_{out} \) – is the amplifiers output power delivered to the load.
- \( P_{DC} \) – is the DC power taken from the supply.

**h**  State the condition for sustained oscillations.  
**Ans:**

**Conditions for sustained oscillations:**
1. The total shift introduced, as the signal proceeds from input terminals through the amplifier and feedback network & back again to the input is precisely 0° or 360°.
2. The magnitude of the loop gain \( A_{V\beta} \) must be equal to 1 at the frequency of oscillations.

\[ A_{V\beta} = 1 & \theta = 0^\circ \text{ or } 360^\circ. \]

<table>
<thead>
<tr>
<th>Attempt any TWO:</th>
<th>8- Total Marks</th>
</tr>
</thead>
</table>
| **a** | **Draw the circuit diagram for Common Base (CB) configuration and draw its input and output characteristics.**  
**Ans:**  
**Circuit diagram for Common Base (CB) configuration:** | **4M** | **2M** |
### Question:

**b** List the types of transistor biasing. Draw neat circuit diagram of voltage divider biasing.

**Ans:**

**Transistor biasing methods:**

1. Base bias / Fixed Bias
2. Base bias with emitter feedback
3. Voltage divider bias/ Self bias
4. Emitter bias

**Circuit diagram of voltage divider biasing:**
c. Draw and explain zener diode as a voltage regulator.

**Ans:**

Circuit diagram:

![Circuit Diagram](image)

**Part I: REGULATION BY VARYING INPUT VOLTAGE:**

A resistance ($R_s$) is connected in series with the zener diode to limit current in the circuit. For proper operation, the input voltage ($V_s$) must be greater than the zener voltage ($V_z$). Where, $R_z = \text{zener resistance}$

$$I_s = I_z + I_L$$

Here the load resistance is kept fixed and input voltage is varied within the limits.

**Case 1:** WHEN INPUT VOLTAGE IS INCREASED

When input voltage is increased the input current ($I_s$) also increases. Thus current through zener diode gets increased without affecting the load current ($I_L$). The increase in input voltage also increases the voltage drop across the resistance $R_s$ thereby keeping the $V_L$ constant.

**Case 2:** WHEN INPUT VOLTAGE IS DECREASED
When input voltage is decreased, the input current gets reduced, as a result of this $I_Z$ also decreases. The voltage drop across $R_s$ will be reduced and thus the load voltage $V_L$ equal to $V_Z$ and load current ($I_L$) remains constant.

**Part II: REGULATION BY VARYING LOAD RESISTANCE**

In this method the input voltage is kept constant whereas load resistance $R_L$ is varied.

**Case 1:- WHEN LOAD RESISTANCE IS INCREASED**

When load resistance is increased, the load current reduces, due to which the zener current $I_Z$ increases. Thus the value of input current and voltage drop across series resistance is kept constant. Hence the load voltage remains constant.

**Case 2:- WHEN LOAD RESISTANCE IS REDUCED**

When load resistance is decreased, the load current increases. This leads to decrease in $I_Z$. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.
### Question 2

**Attempt any FOUR:**

<table>
<thead>
<tr>
<th>Q. No.</th>
<th>Sub Q. N.</th>
<th>Answers</th>
<th>Marking Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>a</td>
<td>Describe the concept of thermal runaway. How it should be avoided?</td>
<td>16- Total Marks</td>
</tr>
</tbody>
</table>

**Ans:**

**Concept of thermal Runaway:**

- We know that $I_C = \beta I_B + (1+\beta)I_{CO}$, where $I_{CO}$ is the leakage current.
- $I_{CO}$ is strongly dependent on temperature.
- The flow of collector current produces heat within the transistor.
- This raises the transistor temperature.
- If no stabilization is done, $I_{CO}$ further increases.
- If $I_{CO}$ increases, $I_C$ increases by $(1+\beta)I_{CO}$
- The increased $I_C$ will raise the temperature of the transistor which in-turn will increase the $I_{CO}$. This effect is cumulative and in a fraction of a second $I_C$ becomes so large causing transistor to burn up. This self-destruction of an unstabilized transistor is known as Thermal Runaway.

**Thermal Runaway can be avoided:**

1. By keeping $I_C$ constant. This is done by causing $I_B$ to decrease automatically with temperature increase.
2. By using heat sink.
<table>
<thead>
<tr>
<th><strong>b</strong></th>
<th>Draw the circuit diagram of two stage RC coupled amplifier. Draw its frequency response.</th>
<th>4M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ans</td>
<td><strong>Circuit diagram of two stage RC coupled amplifier:</strong></td>
<td>2M</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="Circuit Diagram" /></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Frequency response:</strong></td>
<td>2M</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="Frequency Response" /></td>
<td></td>
</tr>
</tbody>
</table>
Explain the working of N-channel JFET with neat diagram.

Ans: N-Channel JFET:

1. The application of negative gate voltage or positive drain voltage with respect to source, reverse biases the gate-source junction of an N-channel JFET. The effect of reverse bias voltage is to form depletion regions within the channel.

2. When a voltage is applied between the drain & source with dc supply voltage ($V_{DD}$), the electrons flows from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current ($I_D$) & its conventional direction is from drain to source. The value of drain current is maximum, when no external voltage is applied between the gate & source & is designated by the symbol $I_{DSS}$.

3. When $V_{GG}$ is increased, the reverse bias voltage across gate-source junction is increased. As a result of this depletion regions are widened. This reduces the effective width of the channel & therefore controls the flow of drain current through the channel.

4. When gate to source voltage ($V_{GG}$) is increased further, a stage is reached at which both depletion regions touch each other as shown in fig (b).

5. At this value of $V_{GG}$, channel is completely blocked or pinched off & drain current is reduced to zero. The value of $V_{GS}$ at which drain current becomes zero is called pinch
off voltage designated by the symbol $V_P$ or $V_{GS(OFF)}$. The value of $V_P$ is negative for N-channel JFET.

d List the types of feedback connection. Draw block diagram representation of them.  

**Ans:**

**Types of feedback connection:-**

1. Positive Feedback

![Positive Feedback Diagram]

2. Negative Feedback

![Negative Feedback Diagram]

**Types of negative Feedback:-**

1. Voltage Series Negative feedback amplifier
2. Voltage Shunt Negative feedback amplifier
3. Current series Negative feedback amplifier
4. Current shunt Negative feedback amplifier

e Draw and explain UJT relaxation oscillator with input and output waveforms.
Ans : 

Circuit diagram and input-output waveform:-

Working principle: -

1. When the supply voltage ($V_{CC}$) is switched ON, the capacitor charges through resistor (R), till the capacitor voltage reaches the voltage level ($V_p$) which is called peak point voltage. At this voltage the UJT turns ON.

2. As a result of this, the capacitor (C) discharges rapidly through resistor ($R_1$). When the capacitor voltage drops to level $V_v$ (called valley point voltage) the uni-junction transistor switches OFF allowing the capacitor (C) to charge again.

3. In this way because of the charging and discharging of capacitor, an exponential sweep voltage will be obtained at the emitter terminal of UJT.

4. The voltage developed at base1($V_{B1}$) terminal is in the form of narrow pulses commonly known as trigger pulses.

5. The sweep period depends upon time constant (RC) and the sweep frequency can be varied by changing value of either resistance (R) or capacitor (C). Due to this fact, the resistor R is shown as a variable resistor. The sweep period is given by the relation

$$T = R.C. \log_e \left( \frac{1}{1-\eta} \right)$$

$$T = 2.3 \ R.C. \ \log_{10} \left( \frac{1}{1-\eta} \right)$$

Ans :

Transistorized Series Voltage regulator:

Draw and explain transistorized series regulator.

Transistorized Series Voltage regulator:
WORKING:-

In above figure, transistor is connected in series with load, therefore the circuit is known as a series regulator.

The transistor behaves as variable resistance whose value is determined by the amount of base current.

\[ V_L = V_Z - V_{BE} \]  

(OR)

\[ V_{BE} = V_Z - V_L \]  

Equation 1

Suppose that value of load resistance is increased. Because of this, the load current decreases and load voltage \(V_L\) tend to increase. From equation (1) that any increase in \(V_L\) will decrease \(V_{BE}\) because \(V_Z\) value is fixed.

As a result of this, forward bias of the transistor is reduced. This reduces its level of conduction. This increases \(V_{CE}\) of transistor which will slightly decrease the input current for the increase in the value of load resistance so that load voltage remains constant.

If the output voltage decreases, then exactly opposite action will take place and output voltage is regulated.

The output of a transistor series regulator is approximately equal to zener voltage \(V_Z\) This regulator can also be used for larger load currents.

<table>
<thead>
<tr>
<th>Q. No.</th>
<th>Sub Q. N.</th>
<th>Answers</th>
<th>Marking Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Attempt any FOUR:</td>
<td>16- Total Marks</td>
<td></td>
</tr>
<tr>
<td>a</td>
<td>Compare CB, CE and CC configuration on the basis of,</td>
<td>4M</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(i) Input Impedance ((R_i))</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(ii) Output Impedance ((R_o))</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(iii) Voltage gain ((A_v))</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(iv) Current gain ((A_i))</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Question b

**Self Biasing Method:**

The self-bias configuration for FET (dc equivalent circuit) is as shown in fig. This configuration eliminates the need of two dc power supplies.

JFET must be operated such that the gate source junction is always reverse biased. This condition requires a negative $V_{GS}$ for n channel JFET. This can be achieved using the self bias arrangement as above –

The resistor $R_G$ does not affect the bias because it has essentially no voltage drop across it and therefore gate remains at 0V. $R_G$ is necessary only to isolate an ac signal from ground in amplifier application.

From above diagram $I_S = I_D$ & $V_G = 0$

$\therefore$ voltage across $R_S = V_{AS} = I_S \cdot R_S = I_D \cdot R_S$

$\therefore V_S = I_D \cdot R_S$

$V_{GS} = V_G - V_S$

$= 0 - I_D \cdot R_S$
**SUMMER– 18 EXAMINATION**
Subject Name: Electronic Devices & Circuits  Model Answer

\[ V_{GS} = - I_D \cdot R_S \]

From Shockley’s equation the drain current is:

\[ I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \]

Substitute the value of \( V_{GS} = - I_D \cdot R_S \)

\[ I_D = I_{DSS} \left[ 1 - \frac{I_D \cdot R_S}{V_{GS(off)}} \right]^2 \]

\[ I_D = I_{DSS} \left[ 1 + \frac{I_D R_S}{V_{GS(off)}} \right]^2 \]

The drain voltage with respect to ground is determined as follows –

\[ V_D = V_{DD} - I_D R_D \]
\[ V_S = I_D R_S \]

The drain to source voltage is –

\[ V_{DS} = V_D - V_S. \]
\[ V_{DS} = (V_{DD} - I_D R_D) - I_D R_S \]
\[ V_{DS} = V_{DD} - I_D R_D - I_D R_S \]

Q point of self Bias circuit is located as –

\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \]

\[ V_{GS} = - I_D R_S \]
\[ I_D = I_{DSS} \left[ 1 + \frac{I_D R_S}{V_{GS(off)}} \right]^2 \]
\[ V_{DS} = V_{DD} - I_D R_D - I_D R_S \]
c) Draw the circuit diagram of double tuned amplifier and describe its working.

**Ans:**

**Circuit diagram:**

```
+-----------------+       +-----------------+
|                 |       |                 |
|    C1            |       |                |
|  +---------------+       |  +---------------+|
|         |                   |         |
|   L1        |                   |   L2        |
| +---------------+                   +---------------+ |
|                 |                   |                 |
|                |                   |                |
|   Cin          |                   |   Cn          |
|  +---------------+                   +---------------+ |
|                 |                   |                 |
|    R1          |                   |    R2         |
|  |             |                   | |             |
|    R2          |                   |    R2         |
|  |             |                   | |             |
|  +---------------+                   +---------------+ |
|                 |                   |                 |
```

**Working:**

When a signal containing many frequencies is applied at the input, the frequency corresponding to the resonant freq. of tuned circuit comprising of $C_1$ & $L_1$ is selected, and other frequencies are rejected. The tuned circuit offers very high impedance to this signal frequency. Amplified output appears across the tuned circuit $L_1 \ C_1$. The output from this tuned circuit is transferred to the second tuned circuit $L_2 \ C_2$ through mutual induction. Frequency response of doubled tuned circuit depends upon the magnetic coupling of $L_1 & L_2$.

A frequency response curve of a typical doubled tuned circuit at different coupling condition is shown –

```
Gain

Loose coupling

Tight coupling

Fr

Frequency
```

From above it is seen that most suitable curve is one when optimum coefficient of coupling exists between the tuned circuits. In this condition, the circuit is highly selective & also provides sufficient amount of gain for a particular band of freq.

Thus by adjusting coupling between two coils the required result can be obtained.
### (frequency response curve is optional. Marks may be awarded even if it is not drawn.)

<table>
<thead>
<tr>
<th>d</th>
<th>Draw pin diagram of IC 723. Give any four important features of IC 723.</th>
<th>4M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ans</td>
<td>Pin diagram of IC 723:</td>
<td>2M</td>
</tr>
</tbody>
</table>

![Pin diagram of IC 723](image)

### Important features of 723:

- It is small in size and less in cost.
- Positive or negative supply operation.
- Unregulated dc supply voltage at the input between 9.5V and 40V
- Output voltage adjustable from 2 V to 37 V.
- Maximum load current of 150 mA
- With additional transistor used, I_{max} upto 10A is available
- Internal power dissipation of 800mW
- Wide variety of applications such as series, shunt, switching and floating regulators.
- Relative simplicity with power supply can be designed.
- Low standby current gain.
- Very low temperature drift
- High ripple rejection.
- Built in fold back current limiting.
- Built in short circuit protection.
- Load and line regulations of 0.03%

### e | Draw and explain transistorized crystal oscillator. | 4M |

---

Page No: 16 / 33
## Ans:
**Circuit Diagram:**

![Circuit Diagram]

**Working:**
When the power is turned on, capacitor $C_1$ is charged. When this capacitor discharges, it sets up oscillations. The voltage across $L_1$ is applied to coil $L_2$ due to mutual inductance. This positive feedback causes the oscillator to produce oscillations. The frequency of oscillations in the circuit is controlled by the crystal. As the crystal is connected in the base circuit its influence on the frequency of the circuit is much more than LC circuit. The entire circuit vibrates at the natural frequency of the crystal. As the frequency of the crystal is independent of temperature, the circuit generates a constant frequency.

## Ans:
**Draw and explain class-B push pull amplifier.**

**Circuit operation:**
When there is no signal, both the transistor $Q_1$ and $Q_2$ are cut off. Hence no current is drawn from the $V_{CC}$ supply. Thus there is no power wasted.

Consider positive half cycle of the input signal the base of $Q_1$ becomes positive and the base of $Q_2$
negative. Therefore $Q_1$ conducts (ON) and $Q_2$ is OFF

When negative half cycle is applied across input, the base of $Q_1$ becomes negative and the base of $Q_2$ is positive. Therefore $Q_1$ is OFF and $Q_2$ conducts. only $i_{c2}$ flows and $i_{c1} = 0$. A negative sinusoidal voltage will appear across load.

Thus at any instant only one transistor will conduct. When $Q_1$ conducts, only $i_{c1}$ flows and $i_{c2} = 0$. A positive sinusoidal voltage will appear across load.

<table>
<thead>
<tr>
<th>Q. No.</th>
<th>Sub Q. N.</th>
<th>Answers</th>
</tr>
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<tbody>
<tr>
<td>4</td>
<td>Attempt any FOUR:</td>
<td>12- Total Marks</td>
</tr>
<tr>
<td>a</td>
<td>Define $\alpha$ and $\beta$ of the transistor. Derive the relationship between $\alpha$ and $\beta$.</td>
<td>4M</td>
</tr>
</tbody>
</table>

**Ans:**

$\alpha$: It is a large signal current gain in common base configuration. It is the ratio of collector current (output current) to the emitter current (input current).

$\beta$: It is a current gain in the common emitter configuration. It is the ratio of collector current (output current) to base current (output current).

**Relation between $\alpha$ & $\beta$:**

\[
\text{Current gain (} \alpha \text{) of CB configuration} = \frac{i_C}{i_E} \\
\text{Current gain of (} \beta \text{) of CE configuration} = \frac{i_C}{i_B}
\]

We know that:

\[
i_E = i_B + i_C
\]

Dividing equation (1) by $i_C$

\[
\frac{i_E}{i_C} = \frac{i_B}{i_C} + \frac{i_C}{i_C} \\
\frac{i_E}{i_C} = \frac{i_B}{i_C} + 1
\]

Therefore \[
\frac{1}{\alpha} = \frac{1}{\beta} + 1
\]

\[
\frac{1}{\alpha} = \frac{1 + \beta}{\beta} \quad [\text{since } \alpha = \frac{i_C}{i_E}, \beta = \frac{i_C}{i_B}]
\]

Therefore \[
\alpha (1 + \beta) = \beta \\
\alpha + \alpha \beta = \beta \\
\alpha = \beta - \alpha \beta \\
\alpha = \beta(1 - \alpha)
\]
Therefore \( \beta = \frac{\alpha}{1 - \alpha} \) OR \( \alpha = \frac{\beta}{1 + \beta} \)

Note: Any other appropriate method for derivation can also be considered and marks awarded.

**b** Compare Class A, Class B, Class C & Class AB power amplifier.  
4M

<table>
<thead>
<tr>
<th>Class</th>
<th>Class A</th>
<th>Class B</th>
<th>Class C</th>
<th>Class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conducts for (360°) full cycle of input signal</td>
<td>(180°) half cycle of input signal</td>
<td>Less than 180° of input signal</td>
<td>Greater than 180° and less than 360°</td>
<td></td>
</tr>
<tr>
<td>Q point is at the centre of load line</td>
<td>On X axis</td>
<td>Below X axis</td>
<td>Just above X axis</td>
<td></td>
</tr>
<tr>
<td>No distortion</td>
<td>More than class A</td>
<td>More than A, B, AB</td>
<td>Less distortion.</td>
<td></td>
</tr>
<tr>
<td>lowest efficiency 25% to 50%</td>
<td>Above 78.5%</td>
<td>Above 95%</td>
<td>Between 50 to 78.5%</td>
<td></td>
</tr>
<tr>
<td>Power dissipation very high</td>
<td>low</td>
<td>Very low</td>
<td>Moderate.</td>
<td></td>
</tr>
</tbody>
</table>

**c** Explain the working of N-channel D-MOSFET.  
4M

**Ans**:

Circuit Operation:

Diagram-2m

Working-2M
The gate to source voltage is set to zero volts by the direct connection from one terminal to the other. & voltage $V_{DS}$ is applied across the drain to source terminals. This results the attraction by the free electrons of the n channel due to positive drain & $I_{DSS}$ establish in the circuit.

For negative voltage at gate, the gate will tend to repel free electrons towards P type substrate and attract holes toward insulated layer. Recombination occurs between electron & holes that will reduce the number of free electron in the channel for conduction. So drain current reduces. The value of voltage of $V_{GS}$ at which drain current nearly becomes zero is called cut off voltage.

When gate is positive with respect to source then positive $V_{GS}$ draws additional electrons from the P type substrate. Thus drain current ($I_D$) increases as increase in positive value.

d) Draw and explain transistor as a switch with neat input and output waveforms.

Ans:

When a sufficient voltage ($Vin > 0.7 V$) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit. The collector current $Vcc/Rc$ flows through the transistor. Therefore switch is ON.

Similarly, when no voltage or zero voltage is applied at the input, transistor operates in cutoff region and acts as an open circuit. Therefore switch is OFF.
In UJT sweep circuit, calculate time period and frequency of oscillation if $\eta = 0.65$ and $R = 2 \, k\Omega$

**Ans:**

$$ t = 2.3RC \log \left( \frac{1}{1-\eta} \right) $$

**Assume** $C = 0.1 \mu F$

$$ t = 2.3 \times 2 \times 10^3 \times 0.1 \times 10^{-6} \times \log \left( \frac{1}{1-0.65} \right) $$

$$ t = 0.2097 \, ms $$

$$ f = \frac{1}{t} $$

$$ f = \frac{1}{0.2097 \times 10^{-3}} $$

$$ f = 4.7687 \, kHz $$

---

**f**

**Draw the block diagram of regulated power supply. State the function of each block.**

**Ans:**

Block Diagram of Regulated power supply:

- **Block Diagram-2M**
- **Function-2M**

Block diagram of a regulated Dc power supply consist of the following blocks namely:

1) Transformer 2)Rectifier 3) Filter 4) Voltage regulator.

1. **Transformer:** The AC main voltage is applied to a step down transformer. It reduces the amplitude of ac voltage and applies it to a rectifier.

2. **Rectifier:** The rectifier is usually centre tapped or bridge type full wave rectifier. It converts the ac voltage into a pulsating dc voltage.

3. **Filter:** The pulsating dc (or rectified ac) voltage contains large ripple. This voltage is applied to the filter circuit and it removes the ripple. The function of a filter is to remove
the ripples to provide pure DC voltage at its output.

This DC output voltage is not a steady DC voltage but it changes with the change in load current. It has poor load and line regulation. The voltage obtained is unregulated DC voltage.

4. Voltage Regulator: The unregulated DC voltage is applied to a voltage regulator which makes this DC voltage steady and independent of variation in load and mains AC voltage. This improves the load and line regulation and provides the regulated DC voltage across the load.

<table>
<thead>
<tr>
<th>Q. No.</th>
<th>Sub Q. N.</th>
<th>Answers</th>
<th>Marking Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Attempt any FOUR:</td>
<td>16- Total Marks</td>
<td></td>
</tr>
<tr>
<td>a</td>
<td>Explain the concept of dc load line analysis.</td>
<td>4M</td>
<td></td>
</tr>
</tbody>
</table>

**Ans :**

**Concept of DC load line:-**

For proper operation of a transistor a fixed level of certain currents and voltage in a transistor are set. These values of current and voltage define the point at which the transistor operates. This point is called operating point. It is also known as quiescent point or simply Q-point.

Consider the transistor circuit shown in the figure above for this circuit we know that the value of collector current is given by the relation.

\[ I_C = \frac{V_{CC} - V_{CE}}{R_C} \]

\[ \text{Equation (i)} \]
Where,

\( V_{CC} \) = The value of DC supply voltage in the collector circuit.
\( V_{CE} \) = The value of collector to emitter, and
\( R_c \) = The Value of collector resistance

The value of collector to emitter voltage (\( V_{CE} \)) at saturation point, is very small as compared to \( V_{CC} \) supply. Therefore the collector current at saturation point is

\[
I_c = \frac{V_{CC}}{R_c}
\]

Equation(ii)

The value of collector current at saturation point designated as \( I_{C(sat)} \) may be obtained by dividing the value of \( V_{CC} \) supply by the value of collector resistance \( R_c \). This value gives us upper end of the load line as shown in the figure.

At cut off point, the value of collector current is zero.

substituting \( I_c = 0 \) in equation(i)

\[
0 = \frac{V_{CC} - V_{CE}}{R_c}
\]

(OR)

\( V_{CE} = V_{CC} = V_{CE(cut\ off)} \).........Equation (iii)

Equation (iii) gives us the lower end of the load line as shown in the above figure.

The region lying in between saturation and cutoff points of the load line is called active region of the transistor operation. Equation (i),(iii) are the Q point coordinates of DC load line.
### Question b

**Draw the circuit diagram of single stage CE amplifier. State the function of each component.**

**Ans:**

**Single stage CE amplifier Circuit diagram:**

![Circuit Diagram](image)

**Function of each component:**

- The potential divider biasing is provided by resistors $R_1$, $R_2$ and $R_E$. It provides good stabilization of the operating point.

- The capacitors $C_1$ and $C_2$ are called the coupling capacitors and are used to pass the AC voltage signals from one side to the other. At the same time, they do not allow the dc voltage to pass through. Hence they are also known as blocking capacitors.
capacitors.

- The capacitor $C_E$ works as a bypass capacitor. It bypasses all the AC currents from the emitter to the ground and avoids the negative current feedback. It increases the output AC voltage.

- The resistance $R_L$ represents the resistance of whatever is connected at the output. It may be load resistance or input resistance of the next stage.

c | Draw drain characteristics of JFET and explain ohmic and pinch-off region. |
--- | --- |
Ans: | Drain characteristics of JFET:

![Drain characteristic curve](image)

**Ohmic Region**: This region is shown as a curve OA in the figure. In this region, the drain current increases linearly with the increase in drain-to-source voltage, obeying Ohm’s law. The linear increase in drain current is due to the fact that N-type semiconductor bar acts like a simple resistor.

**Pinch off region**: This region is shown by the curve BC. It is also called saturation region or constant current region. This means the drain current remains constant at its maximum value (i.e. $I_{DSS}$). The drain current in the pinch off region, depends upon the gate-to-source voltage and is given by the relation...
The above relation is known as Shockley’s equation. The pinch off region is the normal operating region of JFET, when used as an amplifier.

### d. Draw common source FET amplifier and describe its operation.

**Ans:**

**Common source FET amplifier Circuit Diagram:**

![Common source FET amplifier circuit diagram](image)

**Operation of Common source FET amplifier:**

When small a.c. signal is applied to the gate, it produces variation in the gate to source voltage. This results in variation in the drain current. As the gate to source voltage increases, the drain current also increases. As the result of this, the voltage drop across resistor \( R_D \) also increases. This causes the drain voltage to decrease. It means positive half cycle of the input voltage produces the negative half cycle of the output voltage. (ie.) the output voltage is \( 180^\circ \) out of phase with the input voltage.

### e. Construct the circuit diagram of DC regulated power supply for ± 12V using IC 78XX and IC 79XX.

**Ans:**

4 Marks
f) Draw Bootstrap amplifier and describe its working.

Ans:

Bootstrap amplifier:

Here transistor Q₁ acts as a switch and transistor Q₂ acts as an emitter follower (i.e. a unit gain amplifier).

Circuit Operation:
Initially transistor $Q_1$ is ON and $Q_2$ is OFF. Therefore capacitor $C_1$ is charged to $V_{CC}$ through the diode forward resistance ($R_F$). At this instance output voltage is zero.

When negative pulse is applied to the base of transistor $Q_1$, it turns OFF. Since transistor $Q_2$ is an emitter follower, therefore the output voltage $V_0$ is same as base voltage of transistor $Q_2$.

When $Q_1$ turns OFF, the capacitor $C_1$ starts charging capacitor $C$ through resistor ($R$). As a result of these both the base voltage of $Q_2$ and output voltage begins to increase from zero.

As the output voltage increases diode $D$ becomes reverse biased, because of the fact that the output voltage is coupled through the capacitor ($C_1$) to the diode.

Since the value of capacitor ($C_1$) is much larger than that of capacitor ($C$), the voltage across capacitor ($C_1$) practically remains constant.

Thus voltage drop across resistor ($R$) and hence current ($IR$) remains constant, means capacitor $C$ is charged with constant current.

This causes voltage across capacitor $C$ (and hence the output voltage) to increase linearly with time.

The circuit pulls itself up by its own bootstrap and hence it is known as bootstrap sweep circuit.

<table>
<thead>
<tr>
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<tr>
<td>6</td>
<td>Attempt any FOUR:</td>
<td></td>
<td>16- Total Marks</td>
</tr>
<tr>
<td>a</td>
<td>Compare RC coupled, direct coupled and transformer coupled amplifier.</td>
<td></td>
<td>4M</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sr. No</th>
<th>Particulars</th>
<th>RC coupled</th>
<th>Direct coupled</th>
<th>Transformer coupled</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency Response</td>
<td>Excellent in the audio frequency range</td>
<td>Best</td>
<td>Poor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Less</td>
<td>Least</td>
<td>More</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>2</td>
<td>Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Space and weight</td>
<td>Less</td>
<td>Least</td>
<td>More</td>
</tr>
<tr>
<td>4</td>
<td>Impedance matching</td>
<td>Not good</td>
<td>Good</td>
<td>Excellent</td>
</tr>
<tr>
<td>5</td>
<td>Coupling elements</td>
<td>R and C</td>
<td>No element</td>
<td>Transformer</td>
</tr>
<tr>
<td>6</td>
<td>Distortion</td>
<td>Amplitude</td>
<td>No distortion</td>
<td>Frequency</td>
</tr>
<tr>
<td>7</td>
<td>Voltage gain</td>
<td>Least</td>
<td>Less</td>
<td>More</td>
</tr>
<tr>
<td>8</td>
<td>Use</td>
<td>For voltage amplification</td>
<td>For amplifying extremely low frequencies</td>
<td>For power amplification</td>
</tr>
</tbody>
</table>

**b** State the meaning of positive and negative feedback. State four advantages of negative feedback. 4M

**Ans:**

**Positive feedback:** If the feedback signal (voltage or current) is applied in such a way that it is in phase with the input signal and thus increases it, then it is called a positive feedback. It is also known as regenerative feedback or direct feedback.

**Negative feedback:** If the feedback signal (voltage or current) is applied in such a way that it is out of phase with the input signal and thus decreases it, then it is called a negative feedback. It is also known as degenerative feedback or inverse feedback.

**Advantages of negative feedback:**

1. Bandwidth is increased.
2. Noise is decreased
3. Stability is increased
4. Less amplitude and harmonic distortion
5. Less frequency distortion.
6. Input and output resistance can be modified as desired.
7. Less phase distortion

c) Define the terms Line and Load regulation.

**Ans:**

**Line Regulation:** The line regulation rating of a voltage regulator indicates the change in output voltage that will occur per unit change in the input voltage.

Mathematically,

\[
\text{Line Regulation} = \frac{\Delta V_L}{\Delta V_S}
\]

Where \(\Delta V_L\) = the change in output voltage and \(\Delta V_S\) = the change in input voltage

**Load Regulation:**

The load regulation indicates the change in output voltage that will occur per unit change in load current.

Mathematically,

\[
\text{Load Regulation} = \frac{V_{NL} - V_{FL}}{\Delta I_L}
\]

Where \(V_{NL}\) = No load output voltage
\(V_{FL}\) = Full load output voltage
\(\Delta I_L\) = Change in load current demand

d) Draw I-V characteristics of UJT and label different regions on it.

**Ans:**
e) Draw the circuit diagram of fixed bias circuit. Write its working.

Ans:

Applying KVL for the given loop

\[ I_B \cdot R_E + V_{BE} - V_{CC} = 0 \]

or the base current,
\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \] \ldots \ldots \text{Equation (i)}

Since the supply voltage \( V_{CC} \) and the base emitter voltage \( V_{BE} \) have fixed values of voltage, the selection of base bias resistor \( R_B \) fixes the value of base current. Thus the equation (i) may be simplified as

\[ I_B = \frac{V_{CC}}{R_B} \] \ldots \ldots \text{(Since } V_{CC} \text{ is much greater than } V_{BE})

Now consider the collector emitter circuit loop in the base bias circuit and applying the KVL for this loop,

\[ I_C \cdot R_C + V_{CE} = V_{CC} \]

\[ V_{CE} = V_{CC} - I_C \cdot R_C \] \ldots \ldots \text{Equation (ii)}

The above equation gives the voltage drop across the collector emitter terminals of the transistor. The value of collector current is given by

\[ I_C = \beta \cdot \frac{V_{CC}}{R_B} = \frac{V_{CC}}{R_B/\beta} \] \ldots \ldots \text{Equation (iii)}

From above, collector current \( I_C \) is \( \beta \) times greater than base current and is not dependent on resistance of collector circuit (R_C).

\( I_{CE} \) and \( V_{CE} \) are dependent on \( \beta \). But \( \beta \) is dependent on temperature.

It is impossible to obtain a stable ‘Q’ point in a fixed bias circuit.
Because of this fact, base bias is never used in amplifier circuit.

\[ f \] Compare BJT and FET (any four points) \[ 4M \]

\[ \text{Ans : } \]

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Bipolar Junction Transistor(BJT)</th>
<th>Field Effect Transistor(FET)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>It is bipolar device i.e. current in the device is carried either by both electrons &amp; holes</td>
<td>It is unipolar device i.e. current in the device is carried either by electrons or holes</td>
</tr>
</tbody>
</table>
**SUMMER–18 EXAMINATION**

**Subject Name: Electronic Devices & Circuits**  
**Model Answer**

<table>
<thead>
<tr>
<th></th>
<th><strong>It is a current controlled device i.e. the base current controls the amount of collector current.</strong></th>
<th><strong>It is a voltage controlled device i.e. voltage at the gate (or drain) terminal controls amount of current flowing through the device.</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Input resistance is very low compared to FET.</td>
<td>Input resistance is very high</td>
</tr>
<tr>
<td>4</td>
<td>It has a positive temperature coefficient at high current levels. It means that current increases as temperature increases.</td>
<td>It has a negative temperature coefficient at high current levels. It means that current decreases as temperature increases.</td>
</tr>
<tr>
<td>5</td>
<td>It is more noisy.</td>
<td>It is less noisy.</td>
</tr>
<tr>
<td>6</td>
<td>It has higher gain bandwidth product as compared to FET</td>
<td>It has lower gain bandwidth product as compared to BJT.</td>
</tr>
<tr>
<td>7</td>
<td>It is comparatively difficult to fabricate on IC &amp; occupies more space on chip compared to FET.</td>
<td>It is simpler to fabricate on IC &amp; occupies less space on chip compared to BJT.</td>
</tr>
<tr>
<td>8</td>
<td>Transfer characteristics are linear</td>
<td>Transfer characteristics are non-linear</td>
</tr>
<tr>
<td>9</td>
<td>Thermal runaway can damage the BJT</td>
<td>Thermal runaway does not take place</td>
</tr>
<tr>
<td>10</td>
<td>Symbol:</td>
<td>Symbol:</td>
</tr>
</tbody>
</table>